REMARKS

Upon entry of this amendment, claims 1-7, 14, 17, 31, 43, and 54-59 will be pending. Claims 60-64 have been withdrawn. Claims 6, 14, and 58-59 have been amended.

No additional claim fees are believed to be due because there are currently 22 claims including five independent claims. The original filing fees covered 53 total claims including six independent claims.

§ 112 Rejection of Claims 6 and 59

Reconsideration is requested of the rejection of claims 6 and 59 under §112. Claims 6 and 59 have been amended to address the rejection. Applicants therefore request withdrawal of the §112 rejection.

§ 103(a) Rejection of Claims 14 and 54-59

Reconsideration is requested of the rejection of claims 14 and 54-59 as being obvious over Kardos et al. (U.S. 3,956,078) in view of Barstad et al. (U.S. 6,444,110) in light of i) the non-analogous nature of Kardos et al. with respect to the subject matter of claims 14 and 54-59, ii) the absence of any motivation in either reference to make the proposed modification and apply Kardos et al.'s chemistries to semiconductor IC substrates, iii) the lack of any technical basis to expect success, and iv) the improper application of an "obvious-to-try" rationale in support of these obviousness rejections.

Claim 14 is directed to a method for electroplating a copper deposit, which comprises ionic copper as well as a defect reducing agent which reduces the rate of recrystallization and grain growth in the copper deposit, onto a semiconductor integrated circuit device substrate having submicron-sized

reliefs, the method comprising filling the submicron-sized reliefs with the copper deposit such that the deposit is characterized by a reduced concentration of internal voids. Claim 14 has been amended to further require the substrate to include such features with a height-to-diameter aspect ratio of at least 4:1.

Kardos et al.'s relevant substrates are printed circuit boards (PCBs) (Col. 1, line 60), and do not include "semiconductor integrated circuit device substrates." The Kardos et al. method does not pertain to copper filling of interconnects in semiconductor integrated circuit device substrates.

Per MPEP 2141.01(a), a reference may be relied upon as a basis for a section 103 rejection only if it is analogous prior art, which includes references either (1) in the field of the applicants' endeavor or (2) those that are reasonably pertinent to the particular problem with which the applicants were concerned. In this particular instance, the Kardos et al. patent was based on an application filed more than 30 years ago and related to copper plating in the manufacture of PCBs. Printed circuit boards of 30 years ago (and even PCBs of today) are not in the same field as applicants' copper filled vias and trenches of integrated circuits. Printed circuit boards are relatively large substrates that electronic components are mounted onto and then electrically connected to each other by wiring formed by printing copper patterns. Printed circuit boards are typically a resinous material several inches on a side.

In contrast to PCBs, an integrated circuit is a combination of interconnected individual circuit elements inseparably associated with each other within a continuous substrate. An IC

is a semiconductor material such as SiO_2 typically only several millimeters on a side or smaller. Copper is deposited with the goal of completely filling vias and trenches with openings of submicron size, e.g., ***0.5 microns and lower***, which serve as micro, solid-state interconnects between microelements. (Applicants' specification, at ¶0003).

PCBs are resin-based macro-scale carriers of electronic signals between electronic components; whereas ICs are semiconductor-based miniaturized electronic components. These respective substrates are therefore disparate in terms of material properties, character, and function.

Inasmuch as plating of PCBs and filling vias and trenches in ICs are distinct fields of endeavor, therefore, Kardos et al. cannot fairly be relied on under the first analogous art test of MPEP 2141.01(a).

Having failed the first condition under MPEP 2141.01(a), Kardos et al. can only be applied as a basis for rejection under Section 103 if it is "reasonably pertinent to the particular problem with which the inventors were concerned." *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992). In this instance, the problem with which the inventors were concerned was filling submicron sized reliefs, such as vias and trenches, with Cu. In copper filling of vias and trenches it is necessary to "superfill," i.e., deposit Cu into the feature substantially faster in the vertical direction than in the horizontal direction. That is, it is necessary to plate faster from the bottom up than on the feature side walls. Claim 14 has been amended to underscore this "superfilling" aspect of the invention. What is required, therefore, is non-conformal deposition, i.e., deposition which does not conform to the overall shape of the substrate. In contrast, non-conformal

deposition is not an overriding concern in depositing Cu on PCBs. Rather, generally conformal deposition is desired in Cu plating PCBs. In other words, the problem encountered by applicants and others seeking to deposit copper into submicron-sized IC features is to force a deposition mechanism which is substantially faster in the vertical direction than in the horizontal direction. That is "superfilling," a problem about which Kardos et al. were conspicuously silent. This silence, moreover, is understandable in view of the disparate nature of PCBs and IC substrates in terms of character and function. This distinction between the overall goals of the processes -- conformal deposition versus non-conformal superfilling -- is so fundamental that it establishes that Kardos et al. is not "reasonably pertinent to the particular problem [i.e., non-conformal superfilling] with which the inventor was concerned."

As plating copper on PCBs addresses a wholly different set of concerns, one addressing applicants' problem of superfilling submicron-sized features on semiconductor IC substrates would not have reasonably looked to Kardos et al. to provide guidance. The Kardos patent states that the chemistries of the invention "are very suitable for *rotogravure applications, or for the plating of printed circuit boards, or for electroforming* . . ." Contrary to the Office's assertion, Kardos et al. does NOT disclose "copper plating compositions useful to plate circuit board substrates *with small diameter, high aspect ratio microvias and other apertures*" (Office Action, p. 5). These features are only discussed in the Barstad patent, which is discussed in detail below, with respect to modern substrates. Therefore, Kardos et al. cannot fairly be deemed to be analogous art to claim 14 because the problems encountered by Kardos et

al. are not reasonably pertinent to those encountered by the applicants.

Even if the Kardos et al. reference were either in the same field or reasonably pertinent to the same problem as claim 14, Kardos et al. and Barstad et al. do not render the subject matter of claim 14 obvious because there is no suggestion or motivation to make the proposed modification. In the context of establishing a prima facie case of obviousness under §103(a),

> First, there must be ***some suggestion or motivation***, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to ***modify the reference*** or ***to combine reference teachings.*** Second, there must be a ***reasonable expectation of success.*** MPEP 2143, first paragraph.

It is asserted in the Office Action at page 5 that Barstad et al. teach that copper plating compositions useful to plate circuit board substrates with small diameter, high aspect ratio microvias and other apertures will also be useful for plating integrated circuit devices, such as semiconductor devices, relying on Barstad et al.'s text in columns 7 and 8. The applicants respectfully assert that Barstad et al. teach that a ***particular composition*** was found to have benefits with regard to PCB and IC semiconductor substrate technologies. That is, Barstad et al. teach that their composition is useful for plating both types of substrates, but they do not suggest anything about the applicability of any other compositions, such as Kardos et al.'s composition. Barstad et al. state that "a wide variety of substrates may be plated with ***the compositions of the invention.***" The following sentence of the passage elaborates on this statement by stating that "the ***compositions of the invention*** are particularly useful to plate ***difficult work***

pieces, such as ***circuit board substrates with small diameter, high aspect ratio microvias and other apertures . . . [as well as] integrated circuit devices***, such as formed semiconductor devices and the like." Elsewhere in the Barstad et al. patent, it is stated that "a number of improvements in electroplating techniques have been made ***as the articles to be plated [have] evolved in degree of difficulty***" (Col. 1, lines 29-65). Thus, the "difficult work pieces" referred to above can fairly be understood to mean modern substrates.

Based on the asserted utility for the particular composition claimed in the Barstad et al. patent --- the plating of modern PCB and IC semiconductor substrates --- Barstad et al. cannot fairly be deemed to have now broadly made it obvious as a general, sweeping proposition to employ any PCB plating composition whatsoever --- past, present, or future --- for superfilling modern IC semiconductor substrates. That is, Barstad et al. cannot fairly deemed to stand for the broad notion that any copper plating composition that is useful to plate a circuit board substrate will also be useful for plating today's integrated circuit devices, i.e., devices with submicron-sized features, and for solving superfilling problems. Moreover, Barstad et al. make no suggestion, express or implied, that plating chemistries formulated for plating PCBs (whether today or 30 years ago) can be applied successfully to modern semiconductor integrated circuit device substrates. Even granting that "the mere age of . . . references is not persuasive of the unobviousness of the combination of their teachings. . . .[,]"[1] the Barstad patent makes no suggestion to modify Kardos et al. by applying it to IC semiconductor substrates, because the plating chemistries disclosed in Kardos

[1] Applicants acknowledge that the age of the Kardos et al. reference is not disqualifying. But, in combination with Barstad, it does not render claim 14 obvious for the reasons stated herein.

et al. are of no special value for plating IC semiconductor substrates characterized by small diameter, high aspect ratio microvias or other submicron sized reliefs.

Furthermore, there is no basis in either Kardos et al. or Barstad et al. to conclude there is any reasonable expectation of success in applying Kardos et al.'s PCB chemistries to the disparate application of superfilling sub-micron sized features in semiconductor integrated circuit substrates. Barstad et al., while stating that their ***particular*** copper plating compositions can be applied to ***modern*** PCB substrates or semiconductor devices, make no suggestion that any third-party PCB plating composition will be successful for superfilling integrated circuit semiconductor substrates.

Barstad et al. state that "a number of improvements in electroplating techniques have been made as the articles to be plated evolved in degree of difficulty" and that, with regard to semiconductor chips, the "industry ***continually demands*** enhanced performance, including ultra large-scale integration and faster circuits." (Col. 1, lines 29-65). Generally, both the semiconductor chip industry and the printed circuit board industry are regarded as volatile industries, experiencing frequent changes in technology. Thus, as Barstad et al. suggest, improvements in electroplating techniques need to maintain pace with the rapidly changing PCB and semiconductor chip industries. Barstad et al. therefore suggest that older plating chemistries have little or no value in the modern day plating of PCBs and semiconductor devices. Or, at a minimum, they provide no reasonable expectation that a 30-year-old PCB plating chemistry would be successful in superfilling submicron-sized features of IC substrates.

There is simply no basis in either reference, without relying on conjecture, "possibilities or probabilities," or impermissible "obvious-to-try" type logic, to make the technical leap of applying Kardos et al.'s chemistries to IC semiconductor substrates with submicron sized reliefs that require superfilling. Specifically, the MPEP gives as one example of "obvious-to-try" type logic the scenario where it was "obvious-to-try" a "new technology . . . that seemed to be a promising field of ***experimentation***, where the prior art gave only ***general guidance*** as to the particular form of the claimed invention or how to achieve it." MPEP 2145, Section X(B). In this case, the teachings of Kardos et al. are general guidance when viewed in the context of modern, "difficult work pieces" (Barstad, col. 7, lines 56-65), such as semiconductor integrated circuit substrates. As mentioned above, Kardos et al. fail to provide any guidance for addressing the problem with which the applicants were concerned -- filling submicron sized vias and trenches with copper such that the Cu deposit undergoes superfilling, i.e., much faster vertical growth than horizontal growth. Kardos et al. also fail to provide guidance for addressing the problem of the formation of spontaneous internal voids in vias and trenches. While Kardos et al. provide "general guidance" with regard to electroplating a copper deposit onto a substrate, the specific geometries of the applicants' invention and the specific problem of filling copper in a void-free manner are not addressed. Consequently, it would have been, at most, "obvious-to-try" or ***experiment*** with Kardos et al.'s chemistries in regard to IC semiconductor substrates.

In view of i) the non-analogous nature of Kardos et al. with respect to applicants' invention, ii) the absence of any motivation in either reference to make the proposed modification

and apply Kardos et al.'s chemistries to semiconductor IC substrates, iii) the lack of any technical basis to expect success, and iv) the improper application of an "obvious-to-try" rationale in support of these obviousness rejections, applicants respectfully request withdrawal of the rejection of claim 14.

Claims 54-59 depend from claim 14 and are patentable for the same reasons as claim 14 and by virtue of the additional requirements therein.

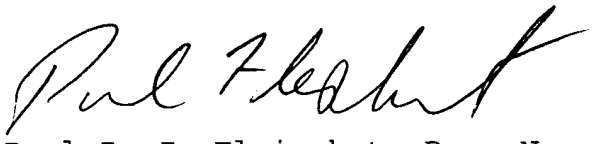
Claims 60-64 Elections/Restrictions

With regard to claims 60-64, which correspond to original claims 15, 16, 18, 19, and 20 and are directed to species which were not elected for examination, these claims stand withdrawn. However, in the event of the allowance of claim 14, which is generic to and readable upon these claims, applicants are entitled to consideration of these claims, which are written in dependent form or otherwise include all the limitations of claim 14. Furthermore, with regard specifically to claim 62, applicants have chosen not to amend it, pending the prosecution of claim 14.

CONCLUSION

In view of the above, allowance of claims 1-7, 14, 17, 31, 43, and 54-59 is respectfully requested.

Respectfully submitted,



Paul I. J. Fleischut, Reg. No. 35,513
SENNIGER POWERS
One Metropolitan Square, 16th Floor
St. Louis, Missouri 63102
(314) 231-5400

PIF/MKG/leb

Express Mail No. EV 455484128 US